ABSTRACT

A clock signal detection circuit is provided that can reliably detect whether or not a clock signal is supplied with a reduced circuit scale and reduced power consumption. The clock signal detection circuit comprises: a tristate buffer circuit that generates an output signal of predetermined potential when a clock signal is in a first level, and that sets the output terminal to the high impedance state when the clock signal is in a second level; a resistor disposed between the output terminal of the tristate buffer circuit and a different potential from the predetermined potential; and a buffer circuit that generates a clock signal detection result in accordance with the output potential of the tristate buffer circuit.